Amendments to the Specification

Please amend line 8 of page 22 of the disclosure as follows:

Patent ~~Application Serial No. 09/314176~~ 6,343,359 (Docket CNTR:1501)

Please amend lines 10-12 of page 19 of the disclosure as follows:

alu-st instructions is described in more detail in ~~co-pending~~ U.S. Patent ~~Application Serial Number 09/313908~~ 6,338,136 (Docket IDT:1503)~~, filed May 18, 1999, and~~ entitled, *PAIRING*

Please amend lines 20-21 of page 34 of the disclosure as follows:

instructions is described in more detail in ~~co-pending~~ U.S. Patent ~~Application Serial Number~~ _____ 6,549,985 (Docket

Please amend line 18 of page 36 of the disclosure as follows:

directly from the E-stage 161 or from the RFC 166, in step 416.

32. (canceled)

33. (original) The method of claim 30, wherein said storehit data comprises a store instruction result within the pipeline having an identical physical store address as said physical load address.

34. (previously presented) A method for speculatively forwarding storehit data in a microprocessor pipeline, the method comprising:

detecting a storehit condition by comparing a load address with a plurality of store addresses;

forwarding storehit data in response to said detecting said storehit condition;

determining said load address is within a non-cacheable address region subsequent to said speculatively forwarding; and

stalling the pipeline in response to said determining said load address is within a non-cacheable address region.

35. (new) A method for speculatively forwarding storehit data in a microprocessor pipeline, the method comprising:

comparing a virtual load address with first and second virtual store addresses, wherein a load instruction specifying the virtual load address is newer than a first store instruction specifying the first virtual store address, which is newer than a second store instruction specifying the second virtual store address;

speculatively forwarding a result of the first store instruction to the load instruction, in response to said comparing indicating the virtual load address matches the first virtual store address and mismatches the second virtual store address;

comparing a physical load address with a physical store address, wherein the physical load address is a translation of the virtual load address, wherein the physical store address is a translation of the second virtual store address;

determining said forwarding the result of the first store instruction to the load instruction was incorrect, after said speculatively forwarding the result of the first store instruction, in response to said comparing indicating the physical load address matches the physical store address; and

forwarding a result of the second store instruction to the load instruction, in response to said determining.

36. (new) The method of claim 35, wherein said comparing the virtual load address with the first virtual store address comprises determining whether the virtual load address hits in a data cache of the microprocessor, wherein said speculatively forwarding the result of the first store instruction to the load instruction comprises the data cache providing the result of the first store instruction to the load instruction.

37. (new) The method of claim 35, further comprising:

stalling the pipeline, in response to said determining, until said forwarding the result of the second store instruction to the load instruction.

38. (new) The method of claim 35, further comprising:

writing the result of the second store instruction to a data cache of the microprocessor, in response to said determining;

wherein said forwarding the result of the second store instruction to the load instruction comprises the data cache providing the result of the second store instruction to the load instruction.

39. (new) The method of claim 35, further comprising:

reissuing the load instruction, in response to said determining.

40. (new) The method of claim 39, wherein said reissuing the load instruction comprises providing the virtual load address to a data cache of the microprocessor from a replay buffer of the microprocessor.

41. (new) The method of claim 35, wherein said comparing the virtual load address with the second virtual store address is performed prior to the result of the second store instruction being stored a store buffer of the microprocessor.

42. (new) The method of claim 35, wherein said speculatively forwarding the result of the second store instruction to the load instruction comprises forwarding the result of the second store instruction from a result forwarding cache (RFC) of the microprocessor.

43. (new) The method of claim 42, further comprising:

caching the result of the second store instruction in the RFC, prior to said comparing the virtual load address with the second virtual store address.

44. (new) The method of claim 43, further comprising:

caching a result of a non-store instruction in the RFC, prior to said comparing the virtual load address with the second virtual store address.